IFW

500.35459VV2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	T. SEKIGUCHI, et al.
Serial No.:	10/810,884
Filed:	March 29, 2004
Title:	METHOD OF MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICES HAVING A MEMORY DEVICE WITH REDUCED BIT LINE STRAY CAPACITY AND SUCH SEMICONDUCTOR INTEGRATED CIRCUIT DEVICES
Group:	2813
Examiner:	Jack S. J. Chen
Confirmation No.:	1085

RESPONSE

Mail Stop: AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

April 11, 2005

SIR:

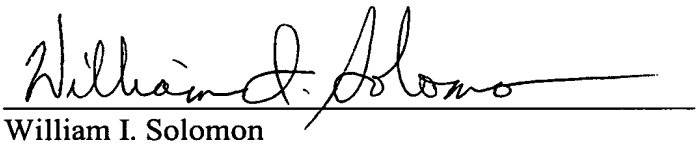
In response to the Office Action mailed March 9, 2005, Applicants respectfully elect Species I (as indicated by the Examiner, Fig. 1), drawn to a method for forming a semiconductor device according to a first embodiment. Pursuant to the additional requirement by the Examiner, it is respectfully submitted that claims 1-6 read on this elected Species I.

Examination of the Species I claims on the merits in the above-identified application, in due course, is respectfully requested.

Applicants request any shortage or excess in fees in connection with the filing of this paper, including extension of time fees, and for which no other form of payment is offered, be charged or credited to Deposit Account No. 01-2135 (Case: 500.35459VV2).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP.



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